REMARKS

Favorable reconsideration of this application is respectfully requested.

The Rejections Under 35 U.S.C. §112

Claim 1 has been amended to particularly point out and distinctly claim the invention. As amended, Claim 1 recites that only the virtualizing aspect of the claimed method occurs without buffering. This avoids the rejection under Section 112, first paragraph. Claim 16 has also been amended to avoid the rejection under Section 112, second paragraph.

In view of these amendments, it is submitted that the rejections under Section 112 are overcome.

The Rejections Under 35 U.S.C. §103

All independent claims except for independent Claim 29 (and independent Claim 19 which was allowed) have been amended; and several of the dependent claims have been amended for consistency with their corresponding independent claims. As amended, all independent claims call for, in somewhat different ways, virtualizing a packet by translating an address of a virtual target to which the packet is destined to an address of a physical target either without buffering the packet or at wire speed.

None of the cited prior art teaches or suggests virtualizing a packet without buffering, as claimed, and the rejections of the claims under 35 U.S.C. §103 on various combinations of U.S. Patent No. 6,880,070 to Gentieu et al., published application U.S. 2005/0111364 to Hipp, U.S. Patent No. 5, 524,254 to Morgan et al.,

U.S. Patent No. 6,693,906 to Tzeng and U.S. Patent No. 6,400,730 to Latif are respectfully traversed.

For the reasons which follow, it is respectfully submitted that the references are not combinable in the manner proposed by the Office, and that the references do not teach or suggest the claimed invention and cannot render the claims obvious.

In particular, no combination of the references teaches or suggests a method, a storage switch, a linecard or software instructions executable by a processor for controlling a switch in which a packet that specifies a virtual target as a destination is virtualized by translating an address of the virtual target to another address of a physical target associated with the virtual target, where the virtualization is performed without buffering the packet or at wire speed, as claimed. Moreover, the teachings of the references would not enable one skilled in the art to make the combinations proposed by the Office.

The Rejection of Claims 1, 2, 7 and 9

The rejection of Independent Claims 1 and 9 over Gentieu in view of Hipp is traversed.

Claims 1, as amended, recites, in relevant part:

> (a) receiving at a first port of the switch a packet that specifies a virtual target as a destination;
>
> (b) sending at a second port of the switch the packet to a physical target that is associated with the virtual target; and
>
> wherein said sending comprises virtualizing said packet by translating a first address of said virtual target to a second address of said physical target without buffering the packet (emphasis added).

Claim 9 is similar except that it recites that the virtualizing occurs at wire speed rather than without buffering the packet.

Gentieu relates to a pipeline network traffic protocol processor for converting data traffic protocols on-the-fly. The processor operates directly on data streams on the processor I/O busses to convert the data protocol on a word basis without requiring the data to be moved in and out of registers or internal memory (col. 2, lns. 51-59). The processor of Gentieu does not comprise a switch, and does not switch a data packet specifying a virtual target to a physical target, as asserted by the Office on page 3 of the Office Action. The reference has nothing to do with virtualizing packets. Rather, the processor generates data for high speed serial data protocols (col. 2, lns 51-53).

Hipp discloses a client - application server computer network having virtual port multiplexing where communications between client computers and application servers that are intended for a physical port are redirected to different virtual ports to avoid interference ([0023], lines 14-16). As described in paragraph [0025], applications, such as a server application, have an associated IP address and an application identifier (AID) which is a network wide unique identifier that corresponds to a specific instant of a running application. Upon receiving a request from a server application on an initial port for a connection, a virtual port multiplexer (VPM) listens for a request from a second application, such as a client application, attempting to connect to the server application at the same IP address and through the same initial port. The VPM allocates, i.e., creates, a second new virtual port to provide a communication path between the server application and the second client application to avoid interference.

This is not the same as translating a virtual target address to a physical target address.

Hipp does not operate on a packet basis, but rather on a connection basis, and does not disclose or suggest either a storage switch or a method that comprises virtualizing packets by translating a virtual target address to a physical target address as set forth in either Claims 1 or 9.

Gentieu and Hipp are directed to quite different and unrelated areas of technology. Nothing in Gentieu or Hipp teaches or suggests combining Gentieu's processor for converting data protocols with Hipp's virtual port multiplexing in a client application server network, and it is respectfully submitted that the teachings of these references are not enabling for the proposed combination and that they could be combined for virtualizing a packet, as claimed.

It is respectfully submitted that the data protocol processor (of Gentieu) has nothing to do with Hipp's VPM for creating virtual ports to avoid interference between two or more clients attempting to access the same physical ports (the opposite of virtualizing a packet, as claimed). Thus, even if the references could be combined as suggested by the Office, the resulting combination would not produce the claimed invention.

Accordingly, since the combination of Gentieu and Hipp teach nothing with regard to virtualizing packets in a storage switch by translating a virtual target address of the packet to a physical target address without buffering the packet or at wire

speed, as set forth in Claims 1 and 9, it is respectfully submitted that the references cannot render these claims or the claims dependent thereon obvious.

Independent Claims 10, 12, 24 and 29-32

As to the rejections of Independent Claims 10, 12, 24, 29, 30, 31 and 32, these independent claims also all recite, in somewhat different ways, translating a virtual target address in a packet to a physical target address without either buffering the packet or at wire speed, similar to Claims 1 and 9. Accordingly these claims, and the claims depending therefrom, are deemed allowable over Gentieu and Hipp for the same reasons discussed above in connection with Independent Claims 1 and 9.

The reference to Morgan, cited for its teaching of linecards, adds nothing to the combination of Gentieu and Hipp with respect to virtualizing packets, as set forth in the independent claims, and does not cure the deficiencies in the teachings of Gentieu and Hipp in this regard.

Claims 10 and 12

Independent Claim 10 is directed to a method for use in a storage switch and recites, in relevant part:

> (b) the first linecard forwarding the packet to a second linecard of the switch along with information about the virtual target, wherein the second linecard includes a port in communication with a physical target associated with the virtual target;
>
> (c) the second linecard utilizing the information about the virtual target to update the packet with an address of the physical target;
>
> wherein steps (b) – (c) comprise translating a virtual target address to said address of the physical target without buffering the packet.

Nothing in Gentieu, Hipp or Morgan teaches or suggests a first linecard of a switch forwarding a packet with information about a virtual target to a second linecard of the switch, the second linecard utilizing the information to update the packet with an address of a physical target, and where these forwarding and utilizing steps comprise translating a virtual target address to a physical target address without buffering the packet, as claimed.

Independent Claim 12 is similar to Claim 10 and the references are inapplicable for the same reasons.

Claims 24 and 29

Independent Claim 24 is directed to a storage switch having a processor that performs a virtualization function to translate a virtual target address to a physical target address for a packet without buffering the packet.

Independent Claim 29 is directed to a storage switch having a plurality of ports on respective linecards, each having a processor unit for receiving a packet destined for a virtual target and including a virtualization unit for translating at wire speed an address in the packet from a virtual target address to a physical target address.

The cited references do not teach or suggestion virtualizing a packet as set forth in these claims.

Claims 30 and 32

Independent Claim 30 calls for a linecard of a storage switch having means for performing a virtualization function to translate a virtual target address to a physical

target address for a packet without buffering the packet. Independent Claim 32 is directed to a storage switch having linecards, and is similar to Claim 30 in calling for means for translating a virtual target address to a physical target address.

These means plus function elements of Claims 30 and 32 must be interpreted pursuant to 35 U.S.C. §112, ¶6 as corresponding to the structure, material and acts disclosed in specification for performing the recited function, and equivalents thereof.

There is no showing in the Office Action of structure, materials or acts in the cited references corresponding to that, or equivalent to that, disclosed in applicant's specification for performing the recited virtualization function in these two claims, and the rejections are improper for this reason alone. Moreover, for the reasons already pointed out, the references do not disclose or suggest virtualizing packets, as claimed, and cannot render Claims 30 and 32 obvious and unpatentable for this reason.

Claim 31

Independent Claim 31 calls for a linecard of a storage switch having a plurality of ports with corresponding processors in which each processor includes "a wire-speed virtualization unit that translates a virtual target address to a physical target address", and that includes virtual target descriptors and physical target descriptors, as claimed. There is no teaching or suggestion in the references of a linecard as set forth in Claim 31, and it is submitted the references cannot render this claim obvious and unpatentable.

Claim 34

Claim 34 is directed to a set of software instructions executable by a processor for performing a series of steps substantially corresponding to the method as set forth in Claim 10, and Claim 34 is deemed allowable over the cited references for the same reasons Claim 10 is deemed to be allowable.

Claims 14, 15, 17 and 18

The rejection of Independent Claim 14, and Claims 15, 17 and 18 as unpatentable over Tzeng in view of Latif is respectfully traversed. (Claim 17 has been cancelled).

Claim 14 has been amended to recite that the ingress linecard retrieving information about a virtual target (step (b) and the egress line card converting a virtual target block address to a physical target block address (step (d)) are performed without buffering a packet.

As previously pointed out in a previous response, the Tzeng patent discloses a layer 2 switch that makes frame forwarding decisions using address and VLAN information in a packet header, where data frames are stored in a buffer memory while processing the frame forwarding decisions for packets (see col. 3, lns. 51 – 67).

The Latif patent teaches a network switch for transferring data between network devices which operate using different data protocols, where input protocols are converted to an internal data format, processed, and then reconverted to an output protocol. Latif teaches buffering of data frames (see col. 15, lns. 14-17).

Both references explicitly teach buffering, and, accordingly, do not teach or suggest the packet virtualizing steps recited in Claim 14. Accordingly, the references cannot render Clam 14 or the claims dependent thereon unpatentable.

In view of the foregoing, it is respectfully submitted that none of the cited prior art teaches or suggests a method for use in a storage switch, a storage switch, a linecard for a storage switch, or software instructions executable by a processor in a storage switch as set forth in Claims 1-18 and 24-35. Accordingly, these claims cannot be rendered obvious and unpatentable by this prior art, and it is respectfully submitted that these claims are allowable.

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Respectfully Submitted,

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